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	P21, remove u504, j502		
	P22, Add 2nd BIOS ROM		
	P23, Change 2x4 PCIE CON+ 2x3 PCIE CON		
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	P25, Change FBVDD uP6205N* 2Phase + SFC choke and uP6262		
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REV	VARIANT	NVPN	ASSEMBLY
B	BASE	600-11025-BASE-SCH	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO. STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	SKU0000	602-11025-0000-300	DT, GF100-050, 659/2000, 1024MB - 32Mx32 GDDR5, DVI-I + DVI-I + mHDMI
2	SKU0001	602-11025-0001-300	DT, GF100-050, 659/2000, 1024MB - 32Mx32 GDDR5, DVI-I + DVI-I + mHDMI
3	SKU0002	602-11025-0002-300	DT, GF100-300, 659/2000, 1280MB - 32Mx32 GDDR5, DVI-I + DP + mHDMI
4	SKU0003	602-11025-0003-300	DT, GF100-030, 659/2000, 1280MB - 32Mx32 GDDR5, DVI-I + DP + mHDMI
5	SKU0004	602-11025-0004-300	DT, GF100-300, 659/2000, 1280MB - 32Mx32 GDDR5, DVI-I + DVI-I + mHDMI
6	SKU0005	602-11025-0005-300	DT, GF100-050, 659/2000, 1024MB - 32Mx32 GDDR5, DVI-I + DVI-I + VENT
7	SKU0006	602-11025-0006-300	DT, GF100-030, 659/2000, 1280MB - 32Mx32 GDDR5, DVI-I + DVI-I + mHDMI
8	SKU0007	602-11025-0007-300	DT, GF100-030, 659/2000, 1280MB - 32Mx32 GDDR5, DVI-I + DVI-I + mHDMI
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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NV PN

600-11025-BASE-SCH

PCB REV

P1025-C00

BOM REV

A

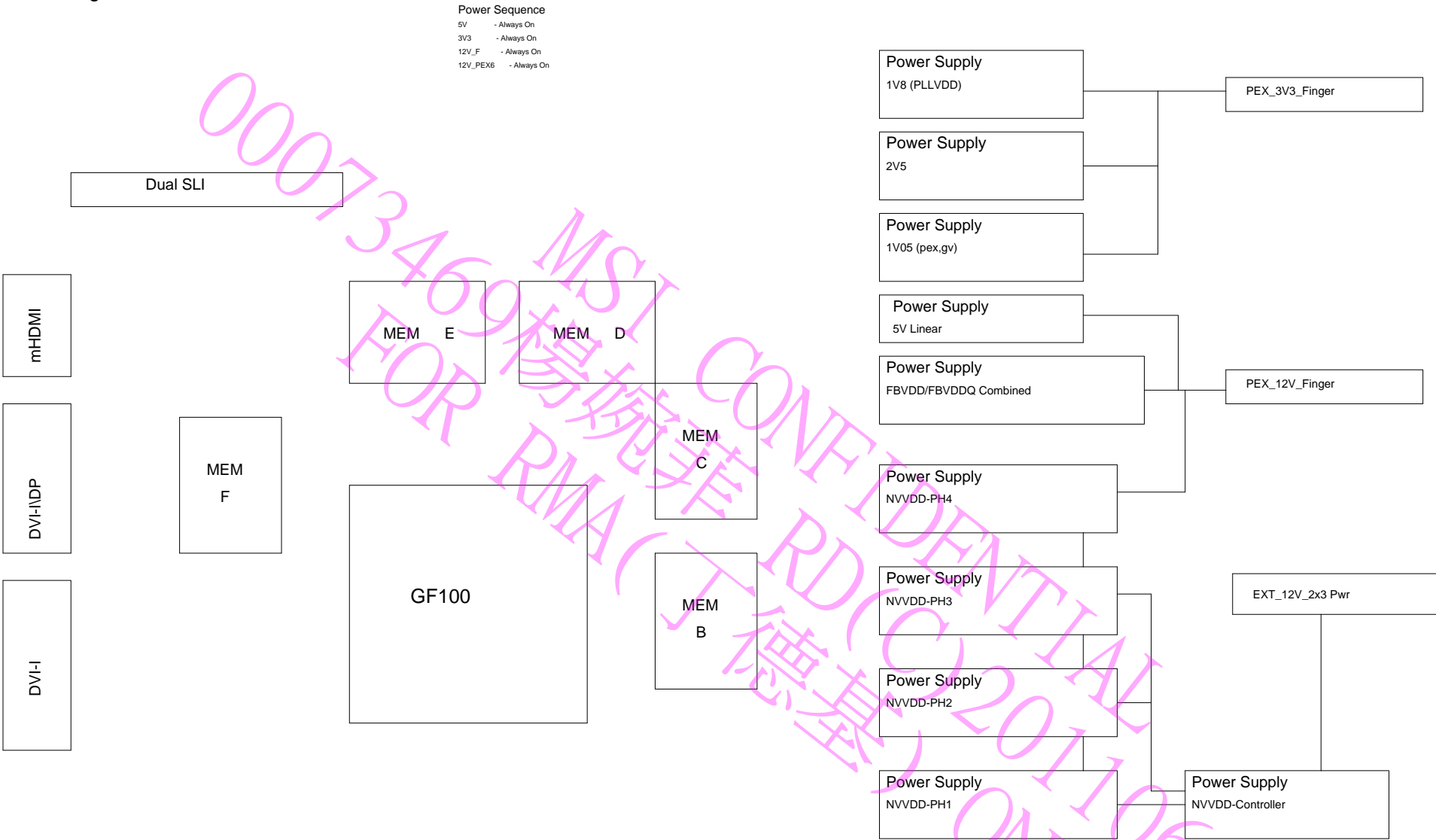
PAGE

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12-JAN-2010



Block Diagram



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PAGE DETAIL	Block Diagram

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PCI Express



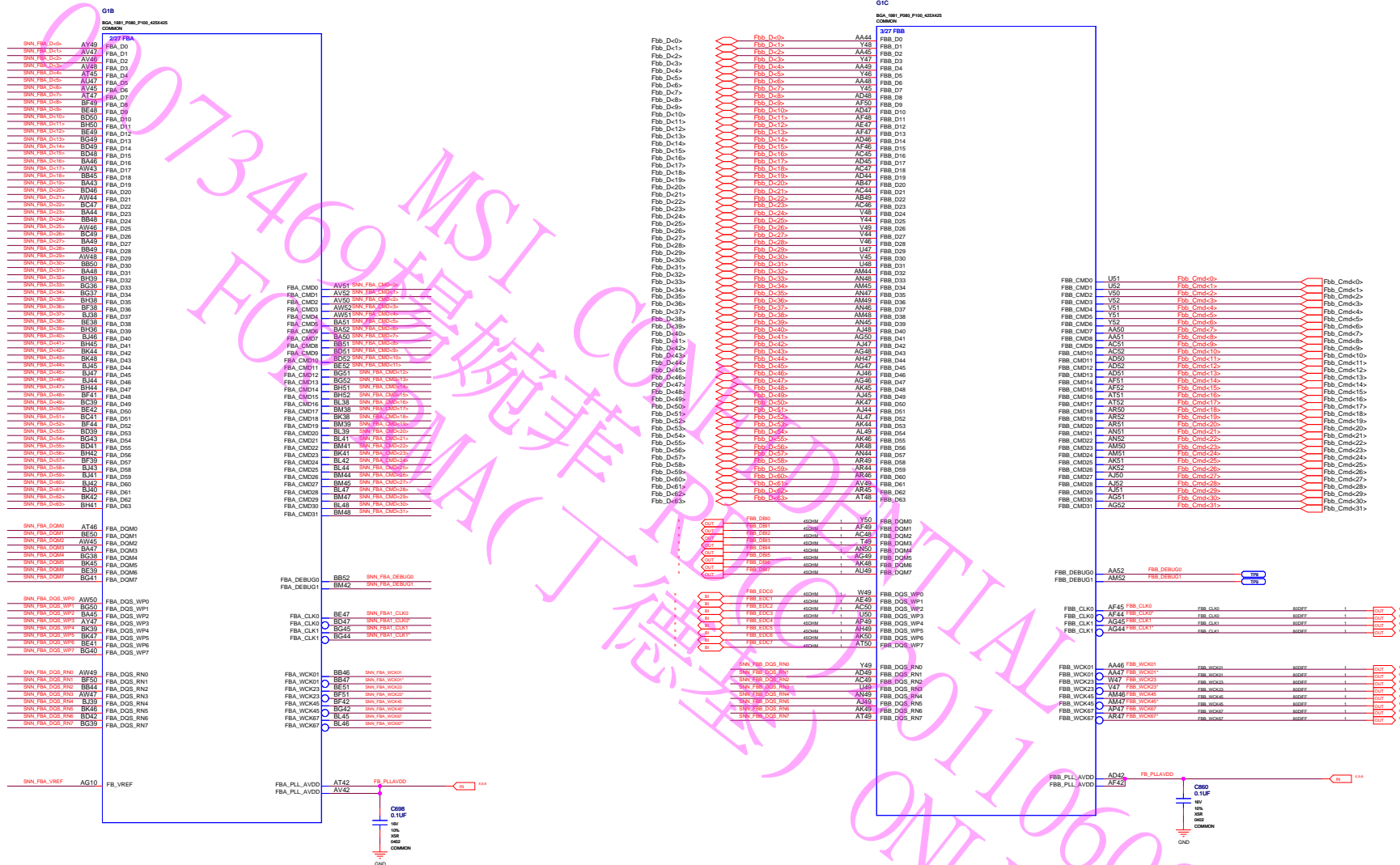
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PAGE DETAIL		PCI Express	
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A	B	C	D
E	F	G	H

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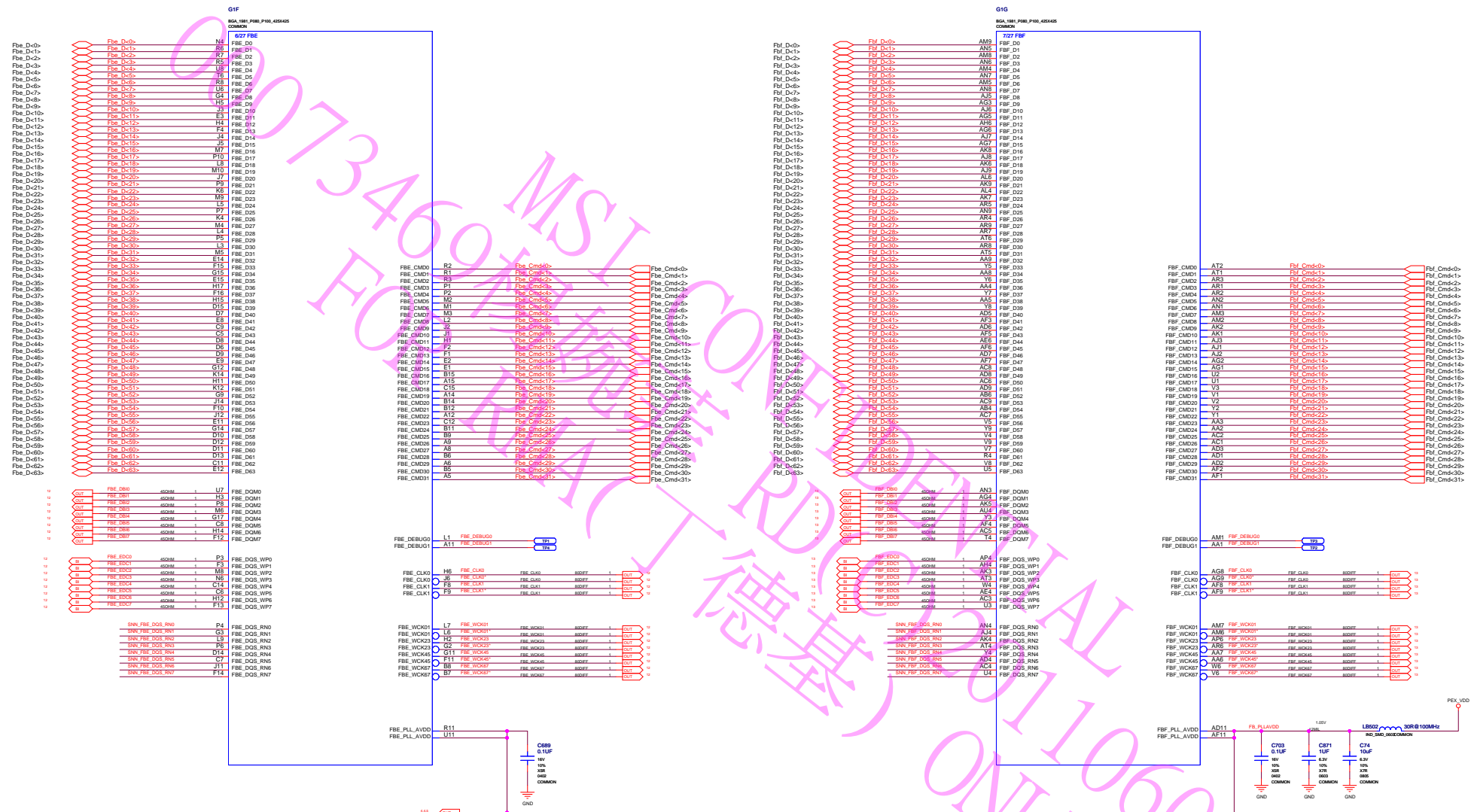
NV_PN 600-11025-BASE-SCH
 PCB REV P1025-C00
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Framebuffer A,B: GPU Section



Framebuffer E,F: GPU Section



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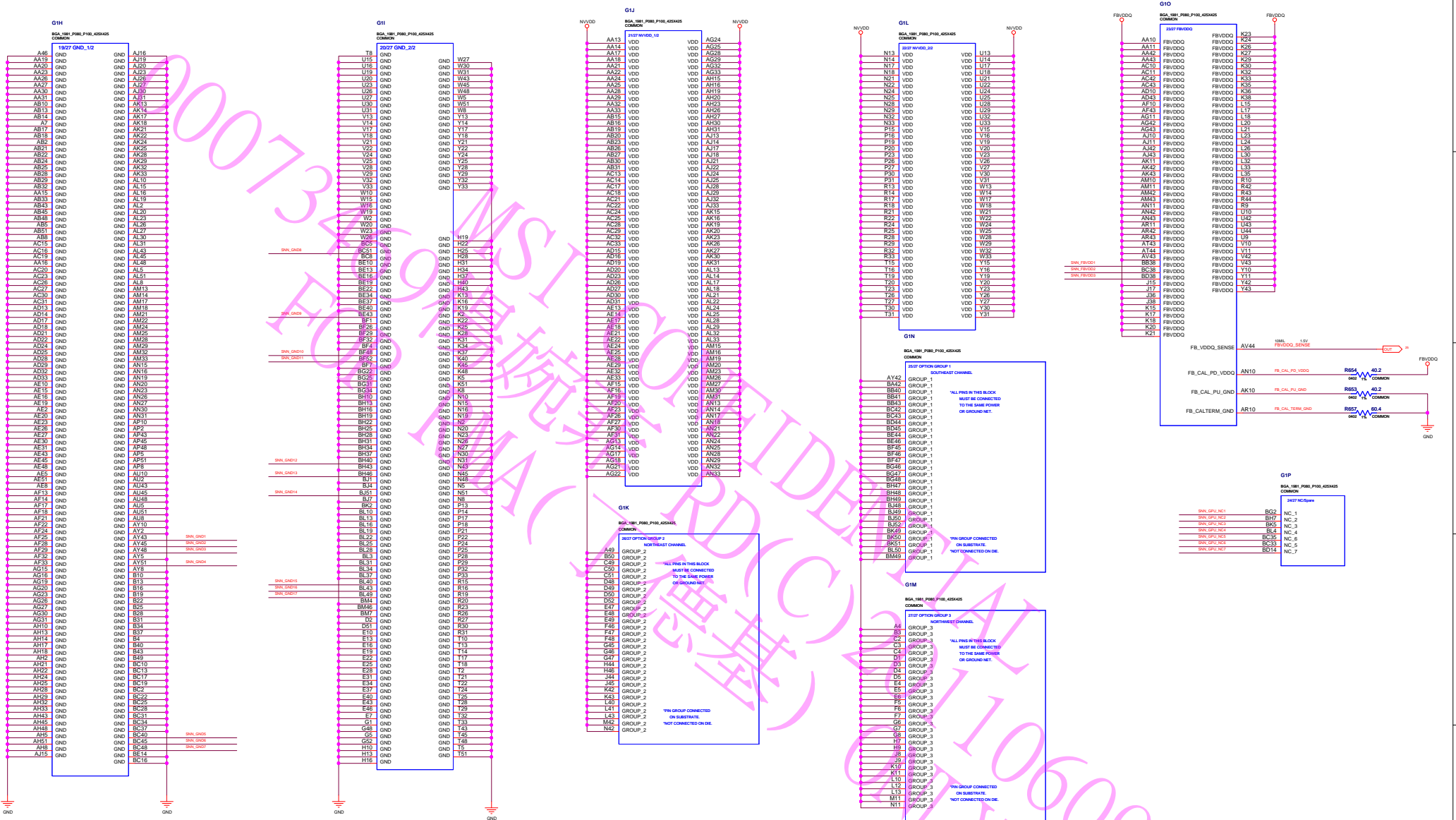
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BOM REV	A
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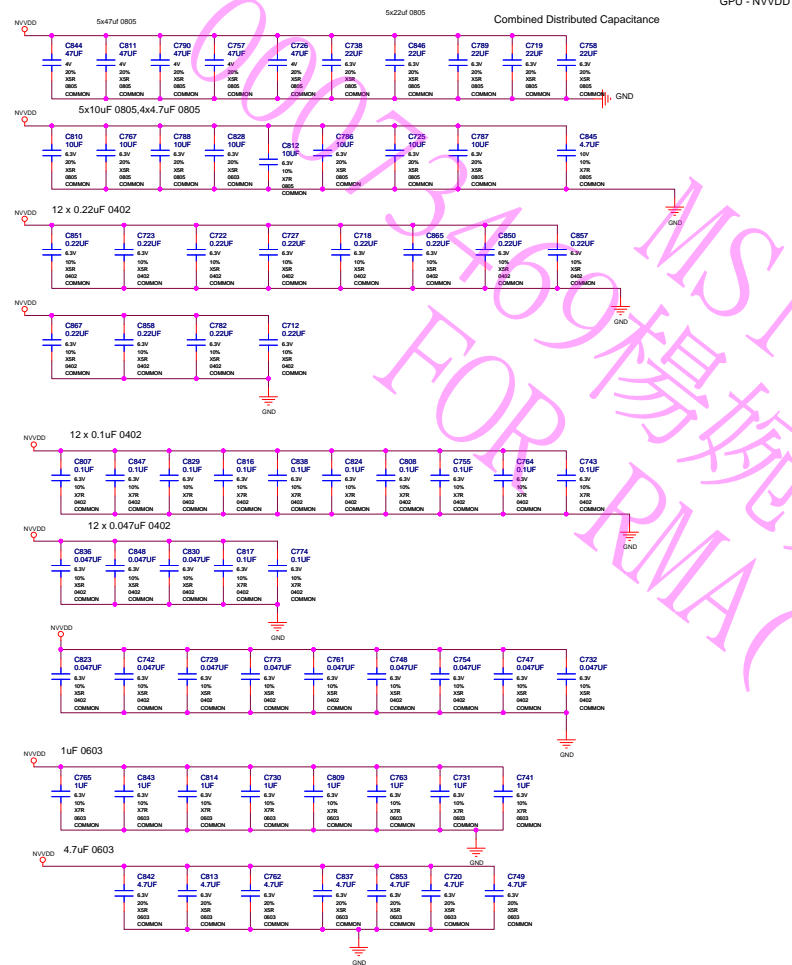
Y

GPU Power and GND

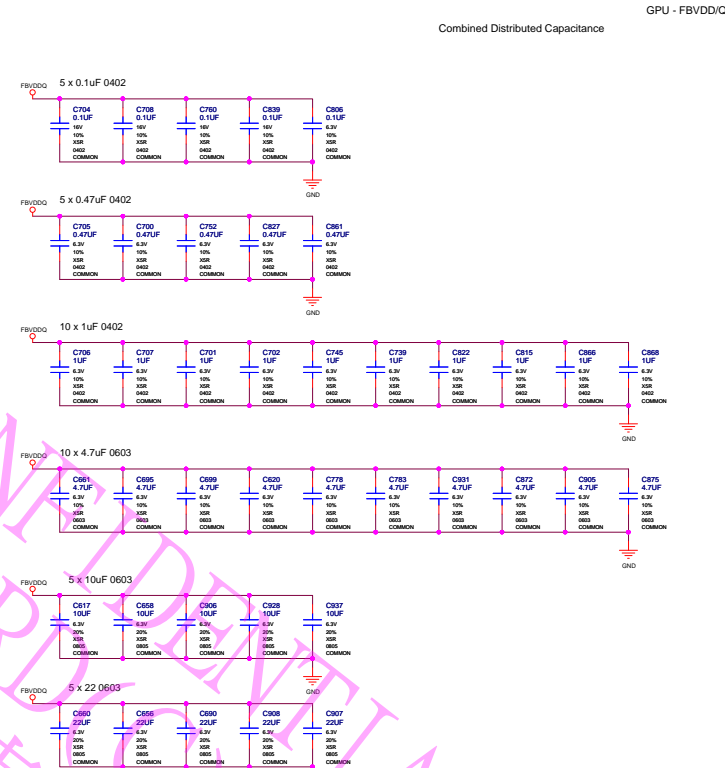


Decoupling: GPU (NVVDD, FBVDDQ)

Decoupling for NVVDD (under GPU)



Decoupling for FBVDDQ (under GPU)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Decoupling: GPU (NVVDD, FBVDDQ)

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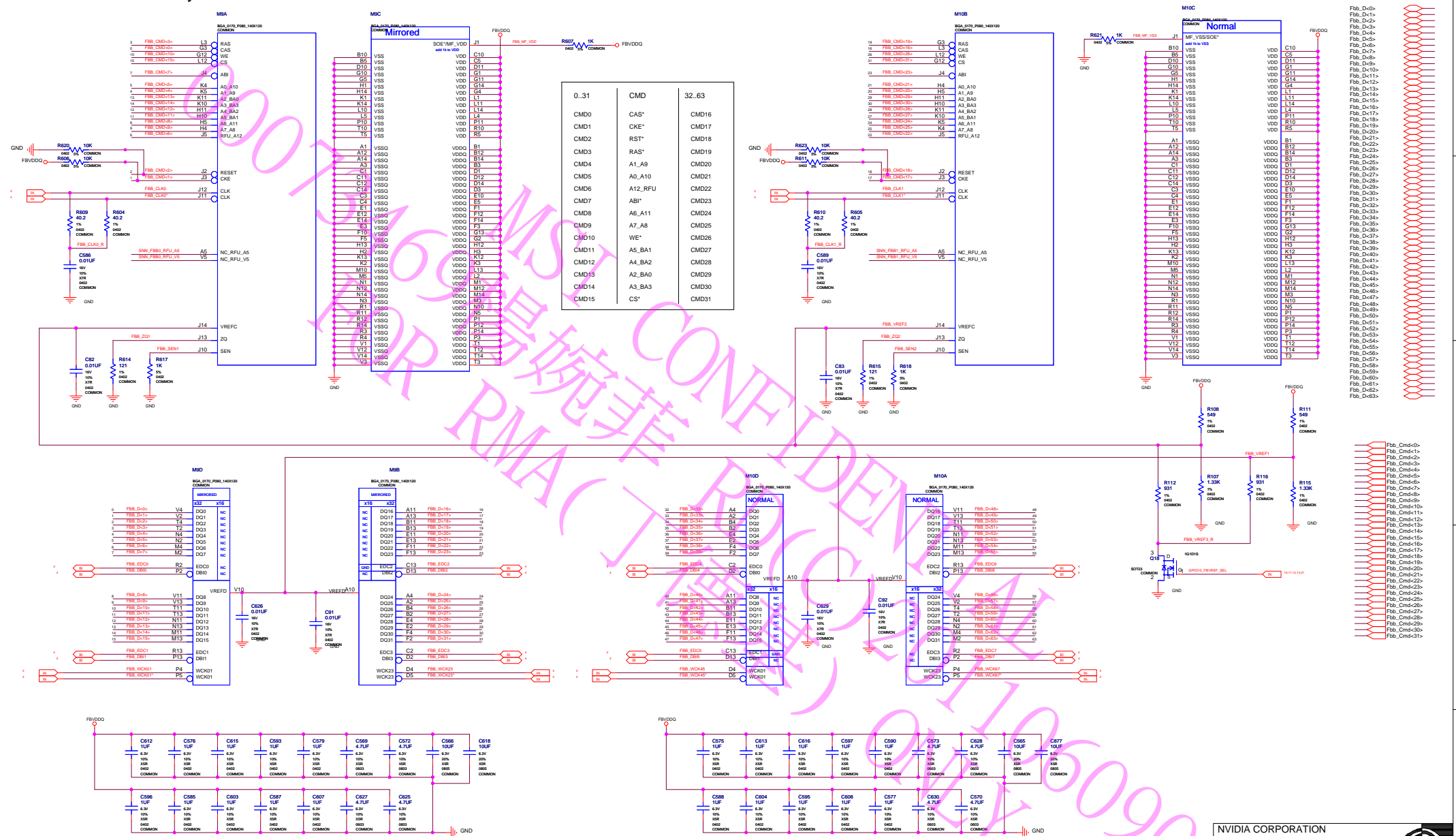


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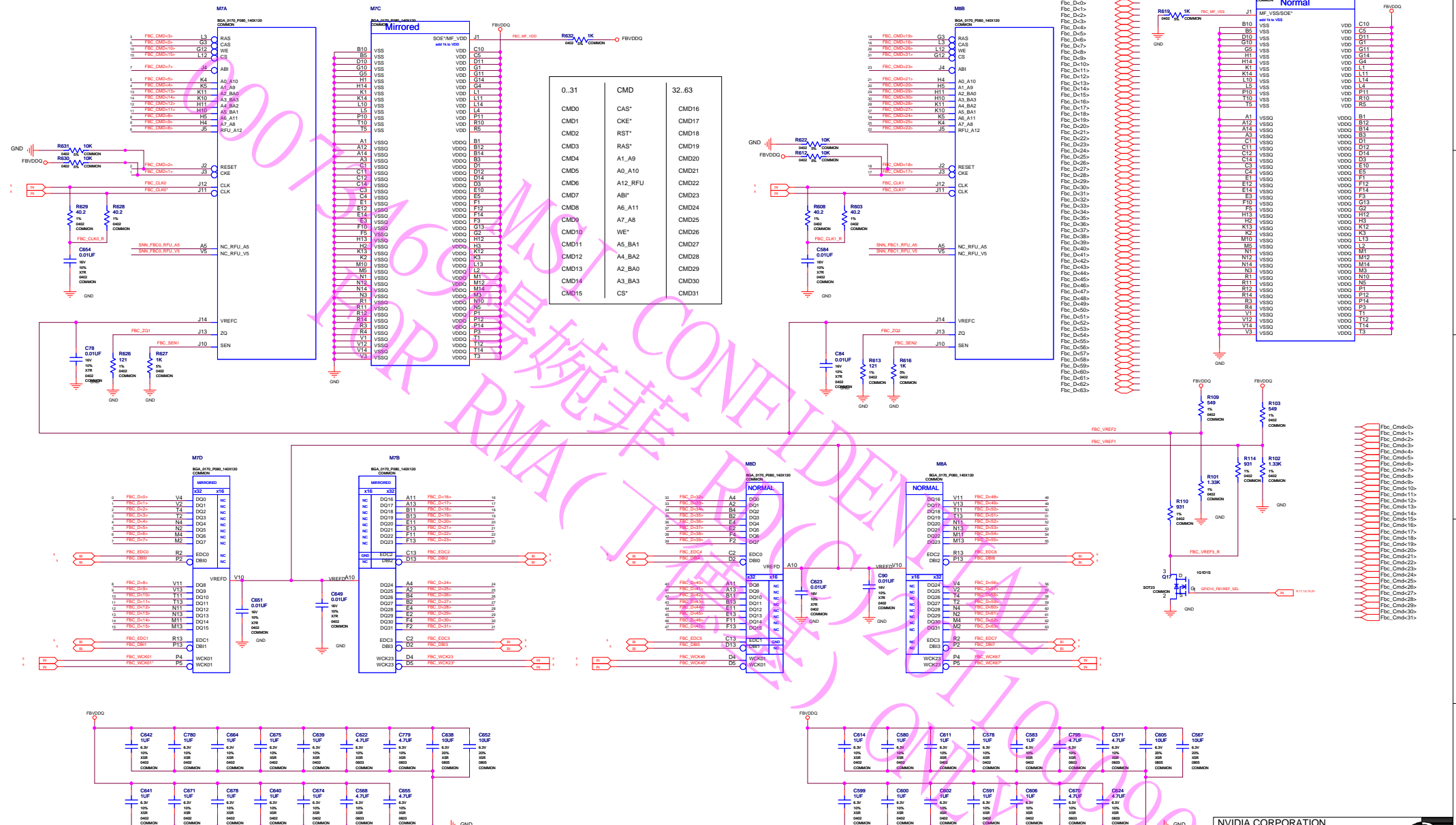
Framebuffer B: Memory Section

Hynix 32MX32 2000MHZ: 161-0063-100
SAMSUNG 32MX32 2000MHZ: 161-0051-600



Framebuffer C: Memory Section

Hynix 32MX32 2000MHZ: 161-0063-100
SAMSUNG 32MX32 2000MHZ: 161-0051-600



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NV_PN 600-11025-BASE-SCH

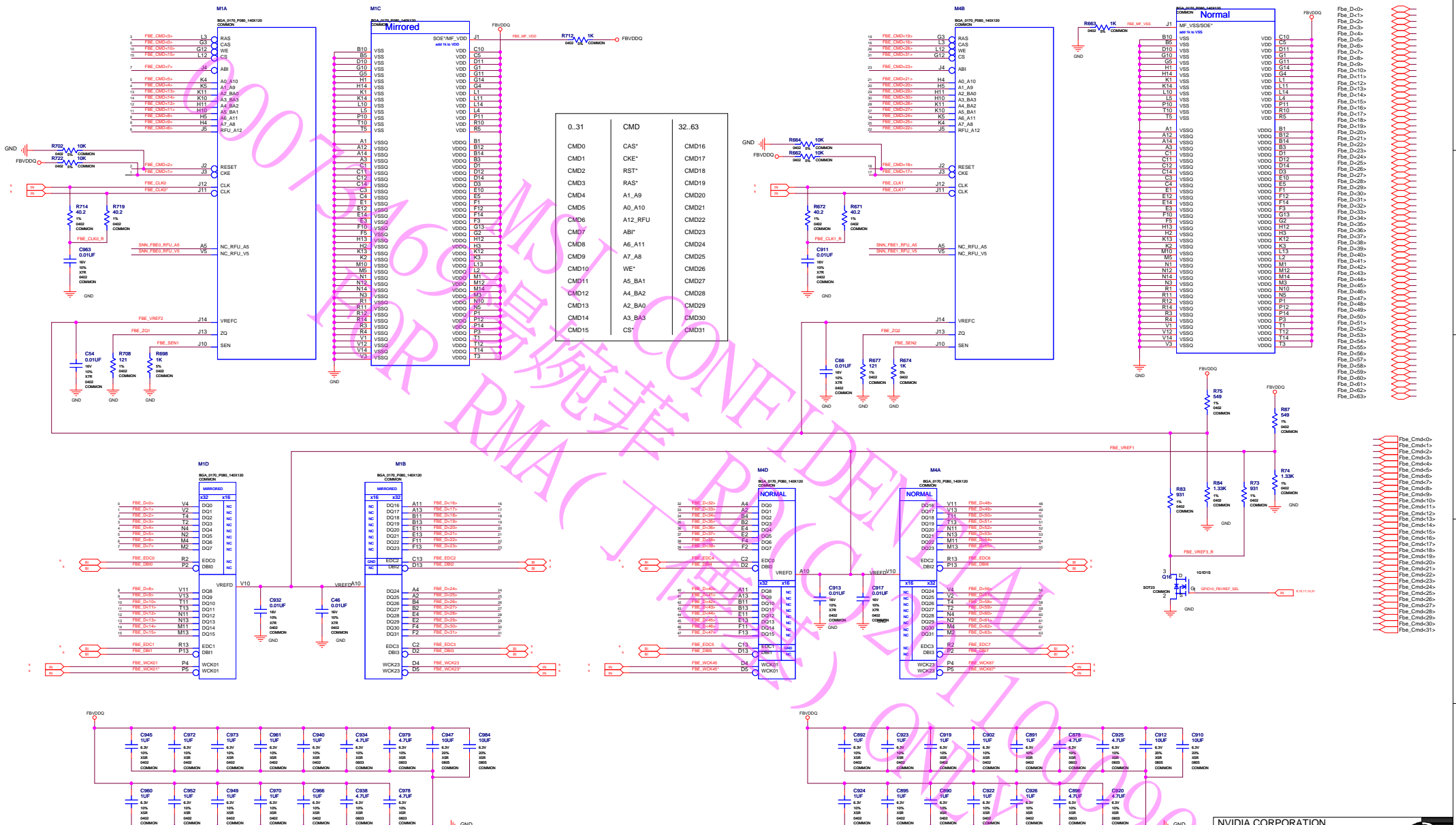
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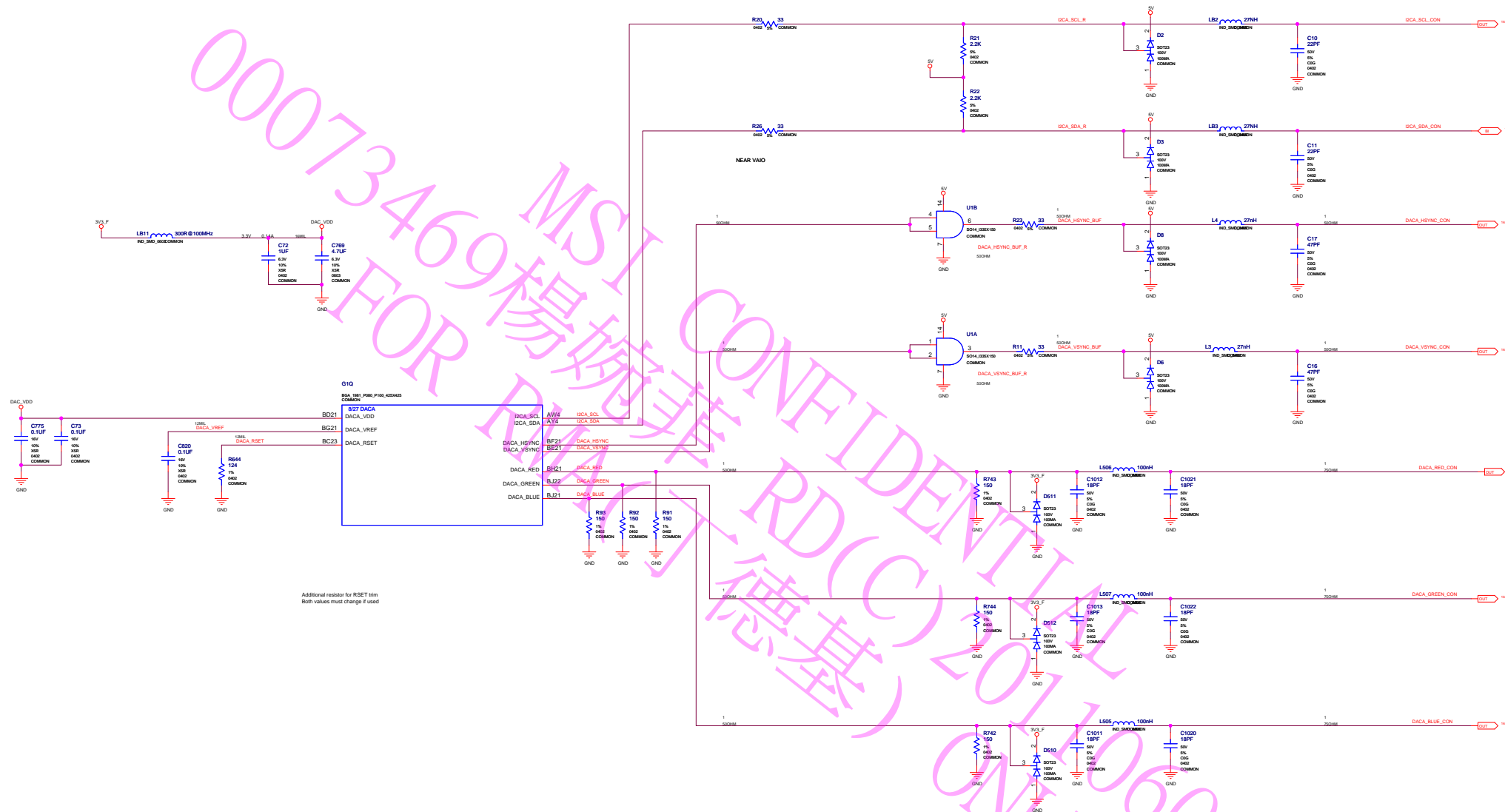
ASSEMBLY BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL Framebuffer C: Memory Section

Framebuffer E: Memory Section

Hynix 32MX32 2000MHZ: 161-0063-100
SAMSUNG 32MX32 2000MHZ: 161-0051-600



Display: DACA (South DVI-I)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Display: DACA (South DVI-I)

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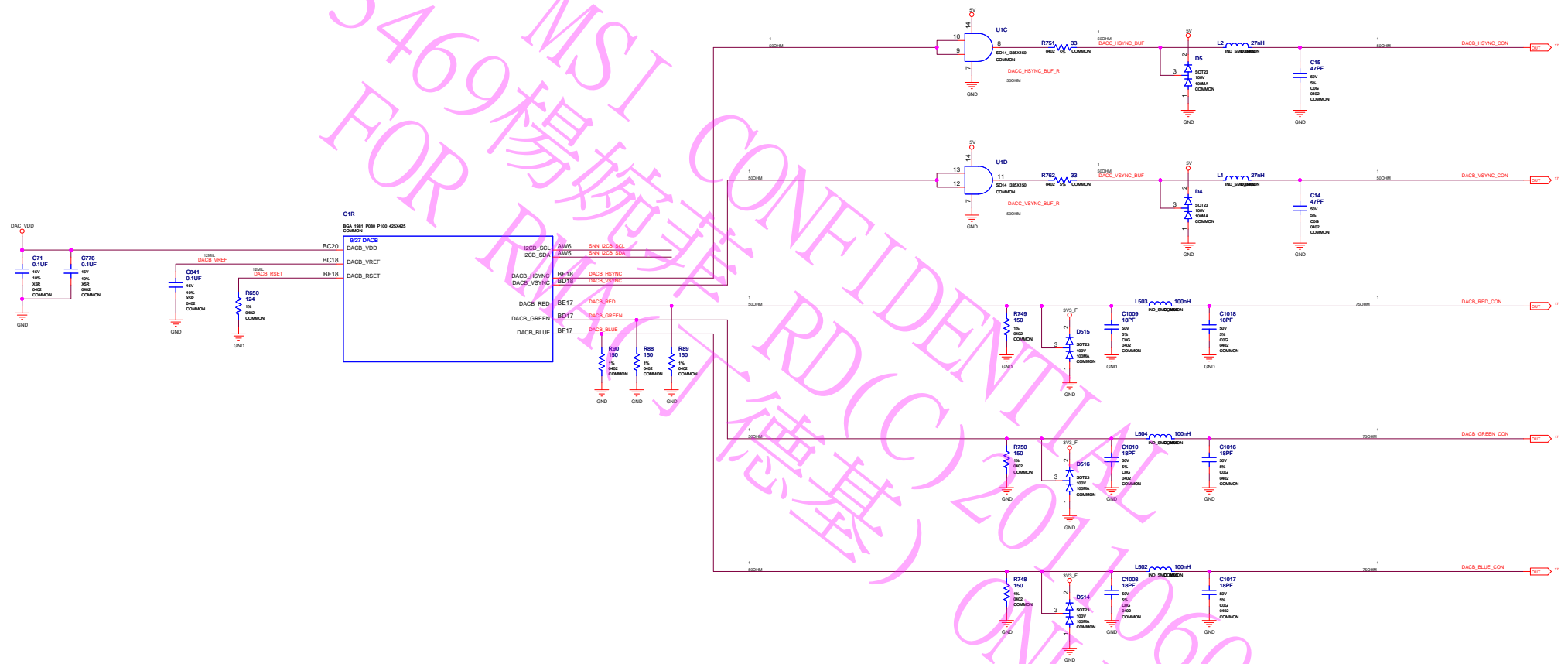
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H

Display: DACB (Middle DVI-I)



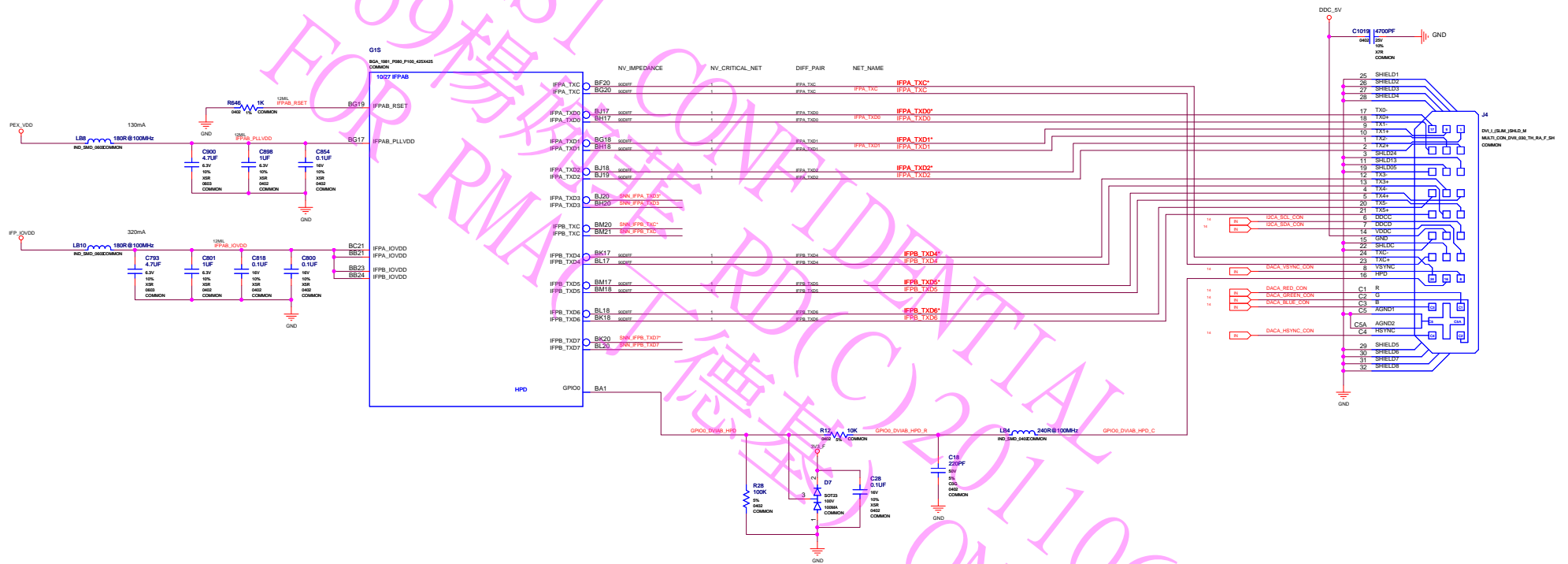
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PAGE DETAIL	Display: DACB (Middle DVI-I)

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IFPAB for South DVI-I (with DACA)

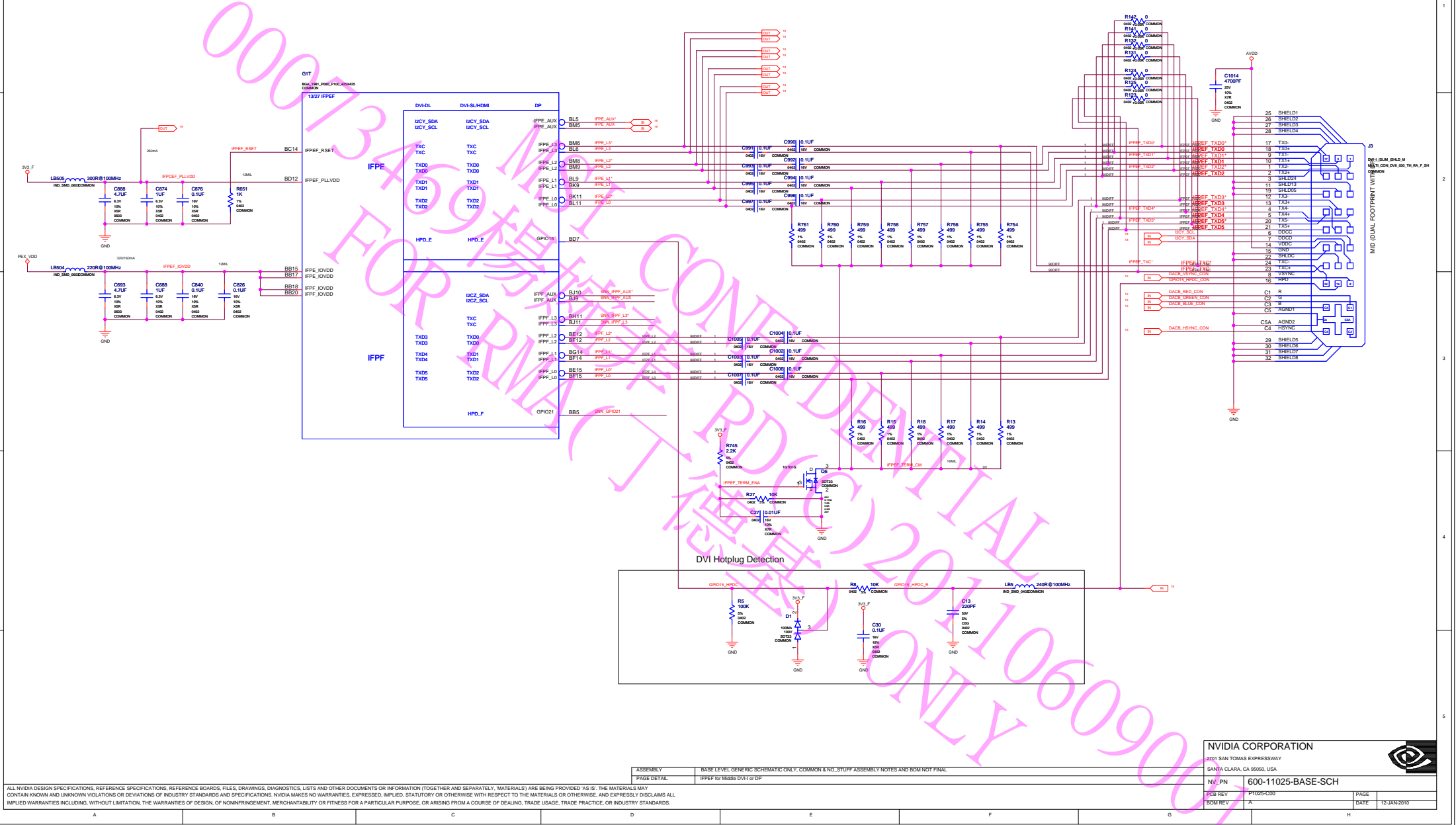


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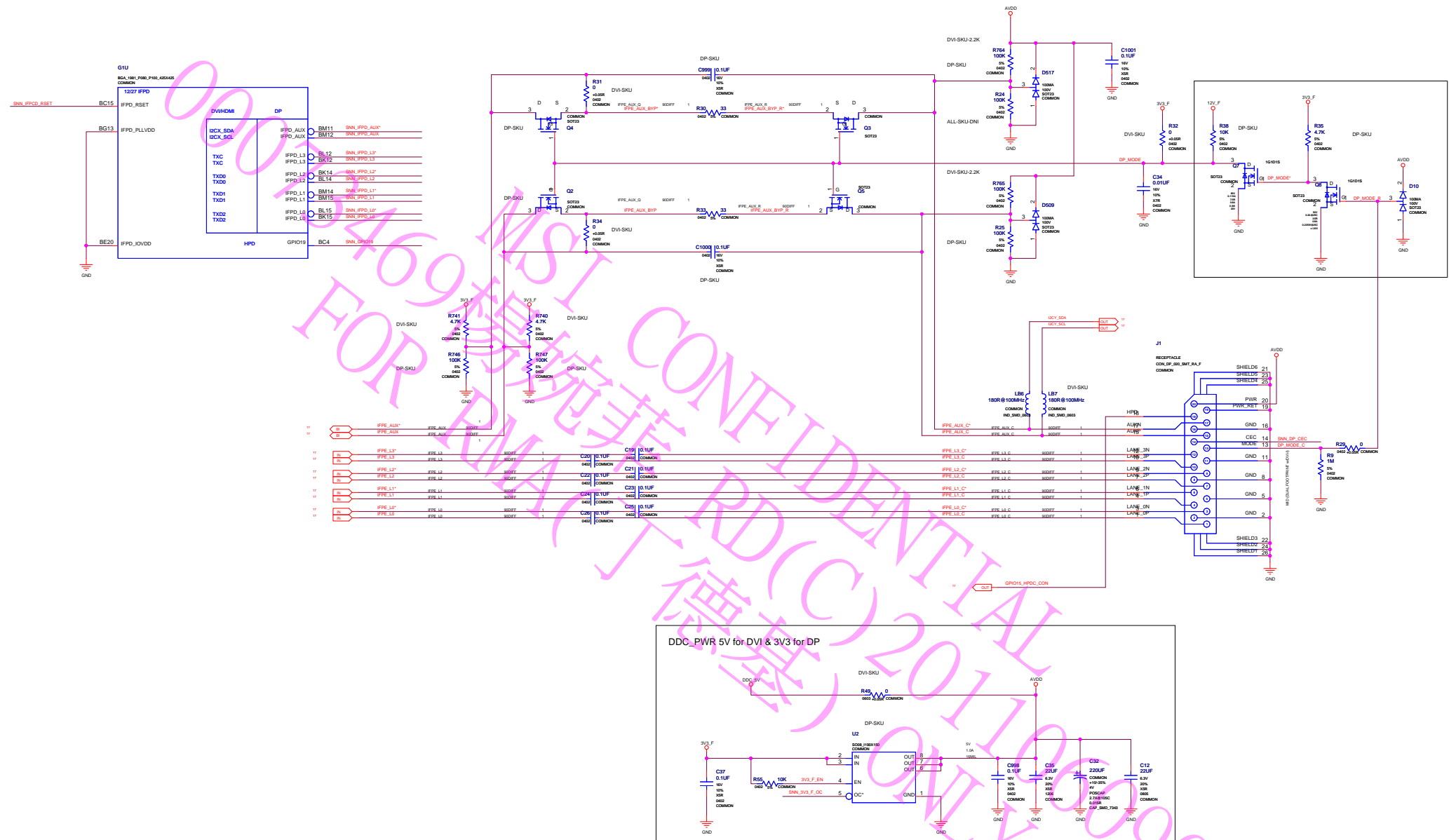
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY; COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	IFPAB for South DVI-I (with DACA)

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IFPEF for Middle DVI-I or DP



IFP_D: UNUSED, (MID DP)



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PAGE DETAIL	IFP_D: UNUSED, (Mid DP)

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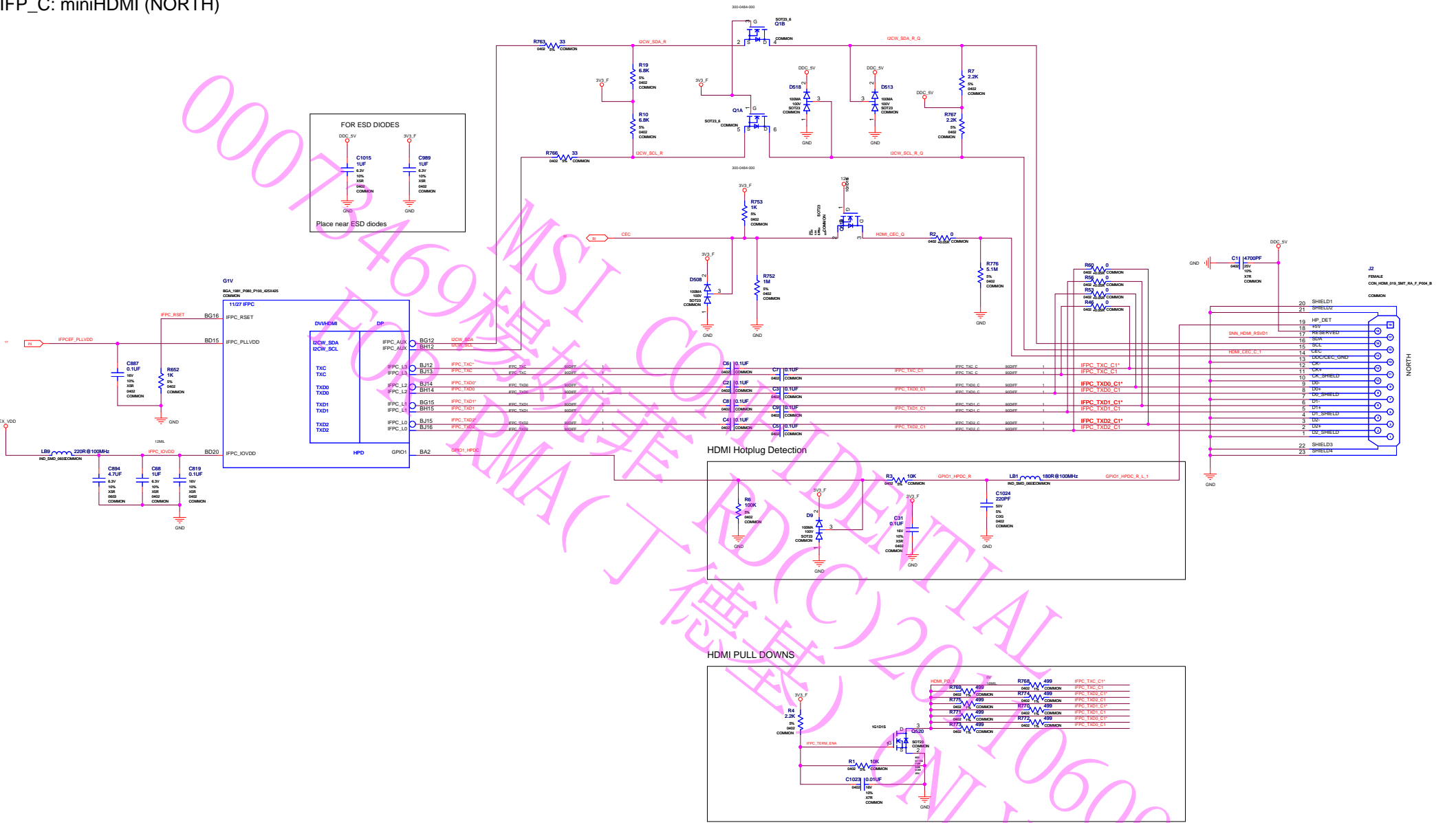
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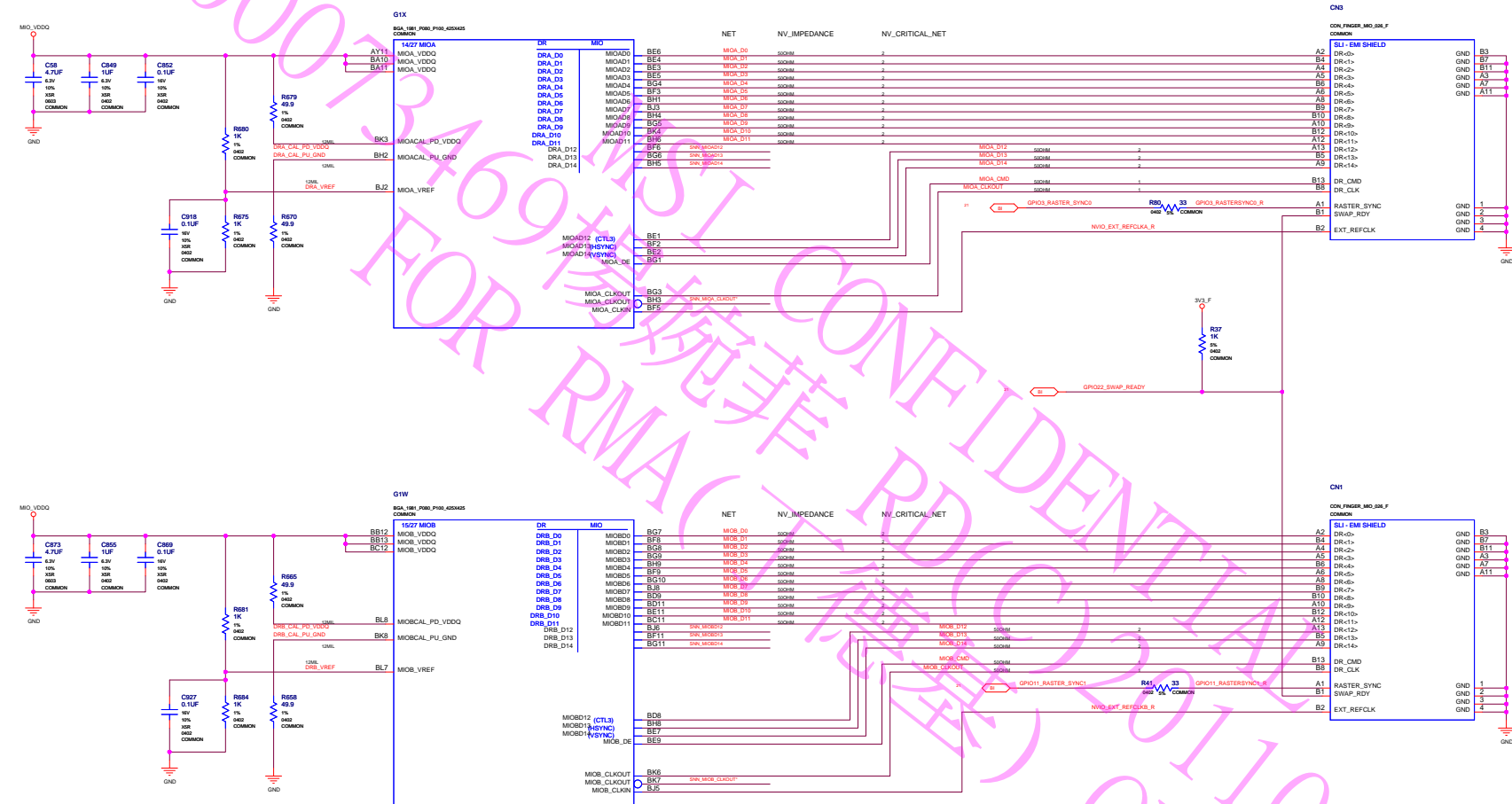
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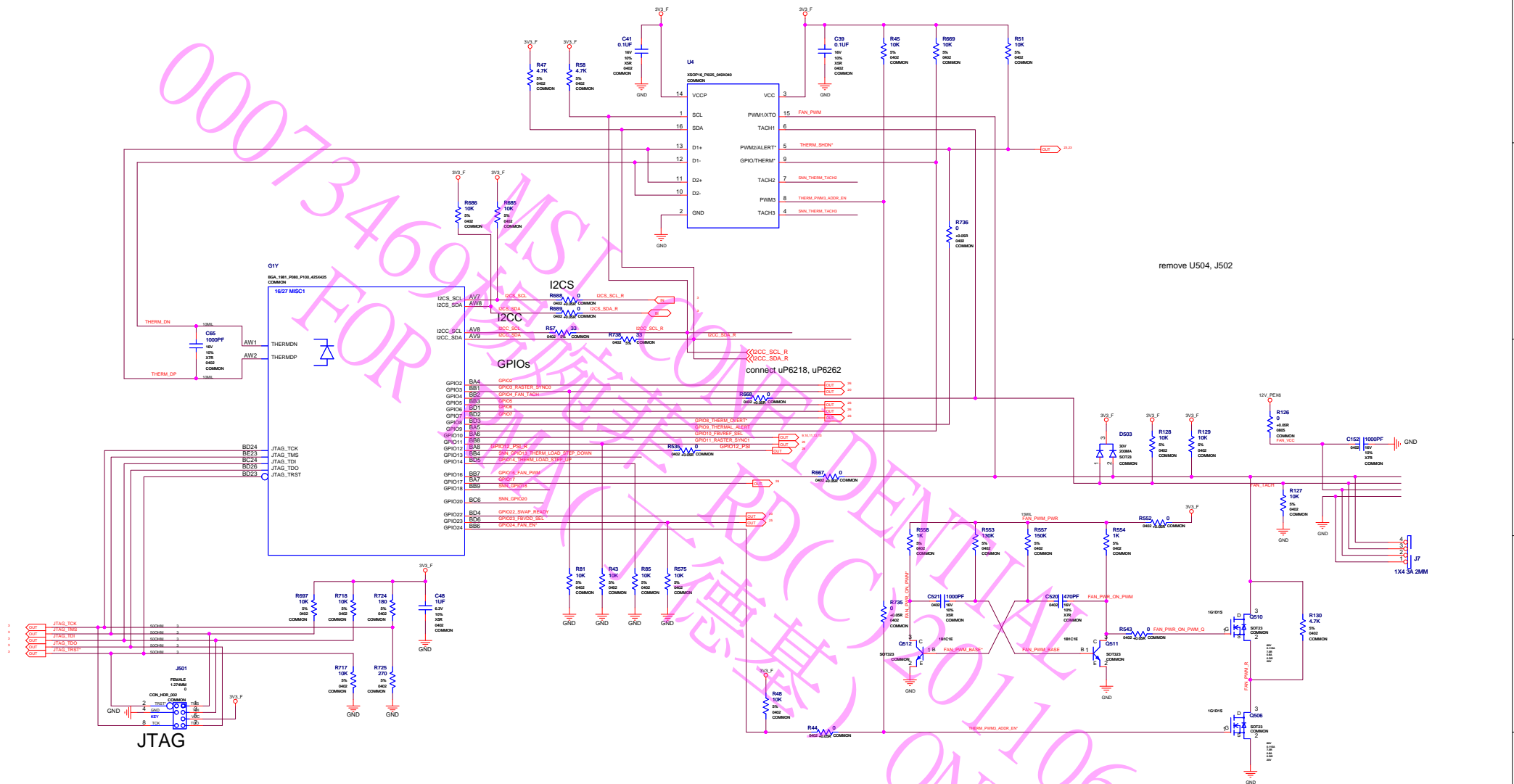
IFP_C: miniHDMI (NORTH)



Connectors: DR Interface (Dual SLI)



FAN CONTROL, GPIO & JTAG



remove U504, J502

JTAG

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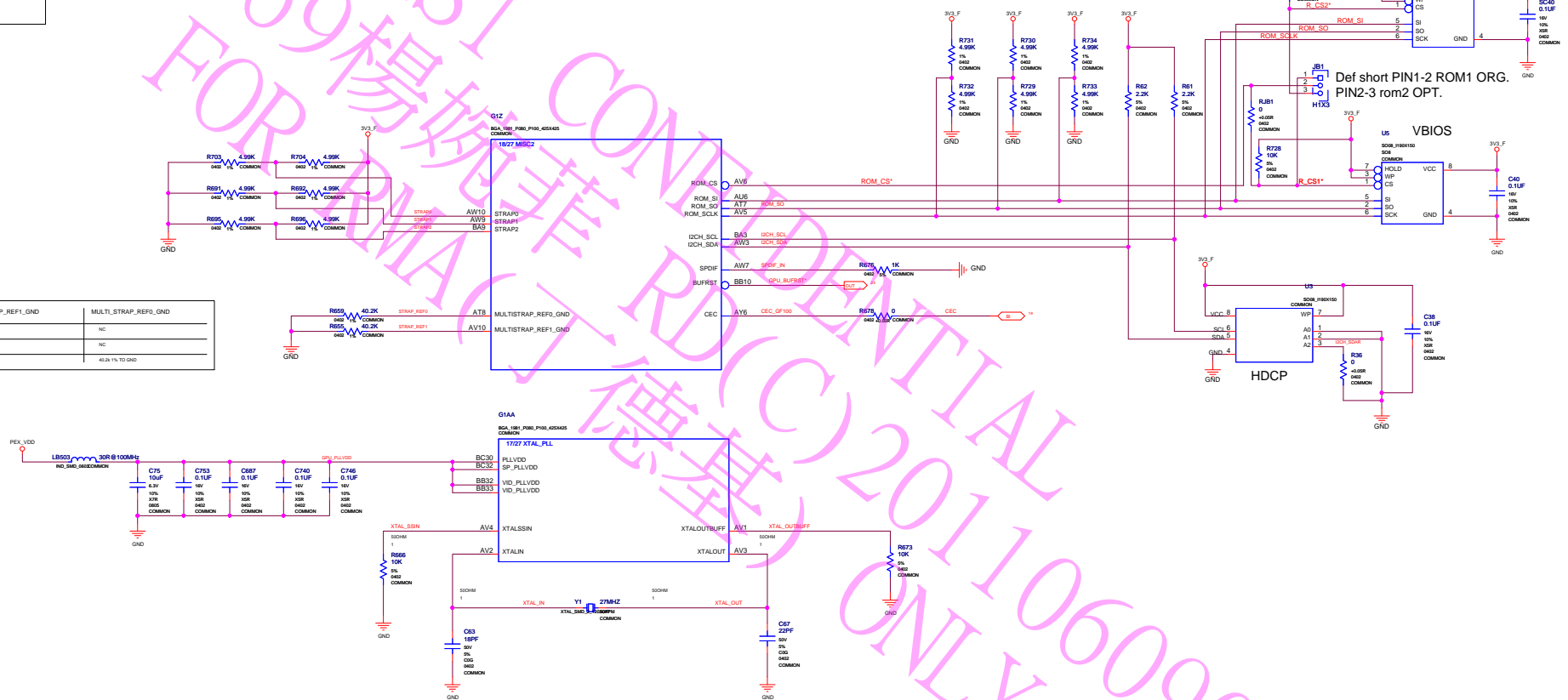
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	FAN CONTROL, GPIO & JTAG


BIOS ROM, HDCP ROM, STRAPPING OPTIONS

STRAP0	USER_BIT [3..0]	0000 => 5K PD	
STRAP1	3GIO_PADCFG_LUT_ADR	0000 => 5K PD	0000 Desktop
STRAP2	PCI_DEVID [3..0]	0000 => 5K PD	For 0x06C0

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

	MULTI_STRAP_REF1_GND	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	40.2k 1% TO GND	NC
BINARY BRINGUP	NC	NC
MULTI-LEVEL	40.2k 1% TO GND	40.2k 1% TO GND



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Power Supply: PEX PS INPUT, DETECTION LOGIC, THERM SHUTDOWN LATCH / IFP_IOVDD

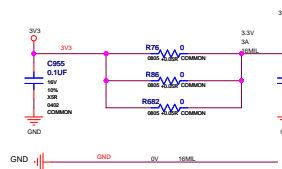
Connector Power State Table

2x3 Connector	Power	STATE
Connected	150W	Full Pwr
Not Connected	75W	Board Off

PEX_12V INPUT - 66W



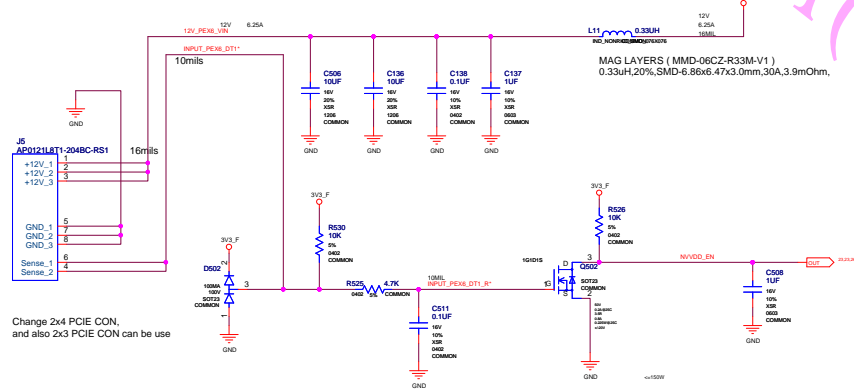
PEX 3V3 INPUT - 10W



MUST BE ATTACHED AND POWERED TO START BOARD

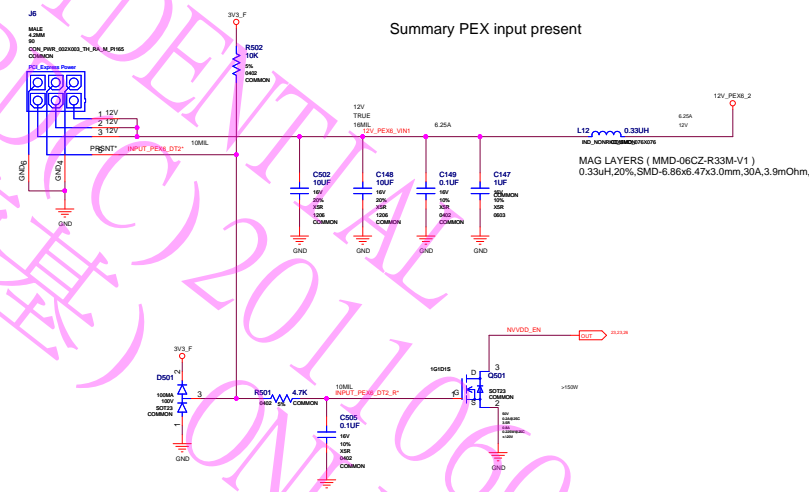
PEX6 INPUT 1 - 2x3 PCIE CON 75W

Summary PEX input present



Change 2x4 PCIE CON,
and also 2x3 PCIE CON can be use

Summary PEX input present



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PAGE DETAIL	PEX PS INPUT, DETECTION LOGIC, THERM SHUTDOWN LATCH / IFP_IOVDD

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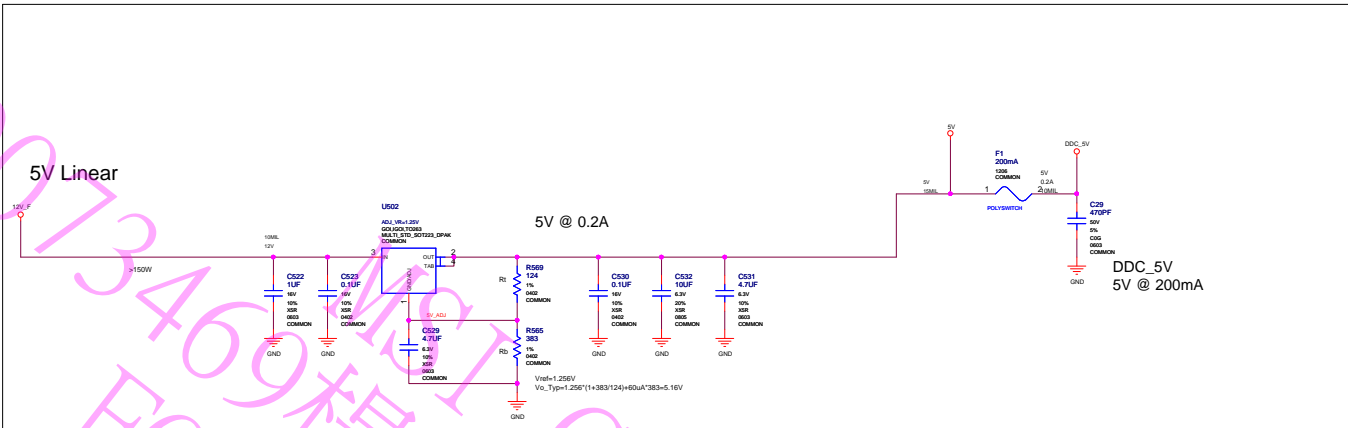
NV_PN 600-11025-BASE-SCH

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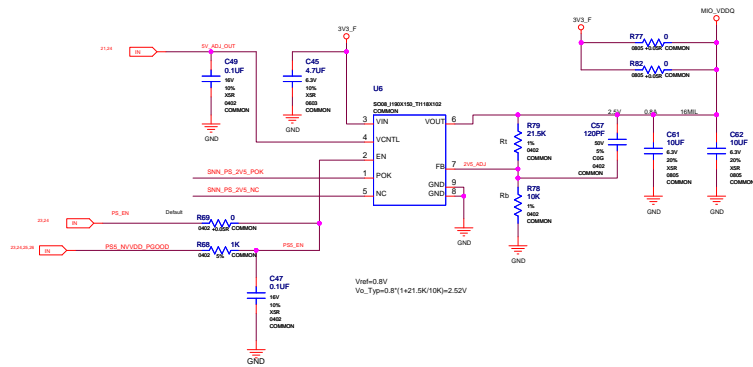
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Power Supply: 2V5,5V, PEX_VDD



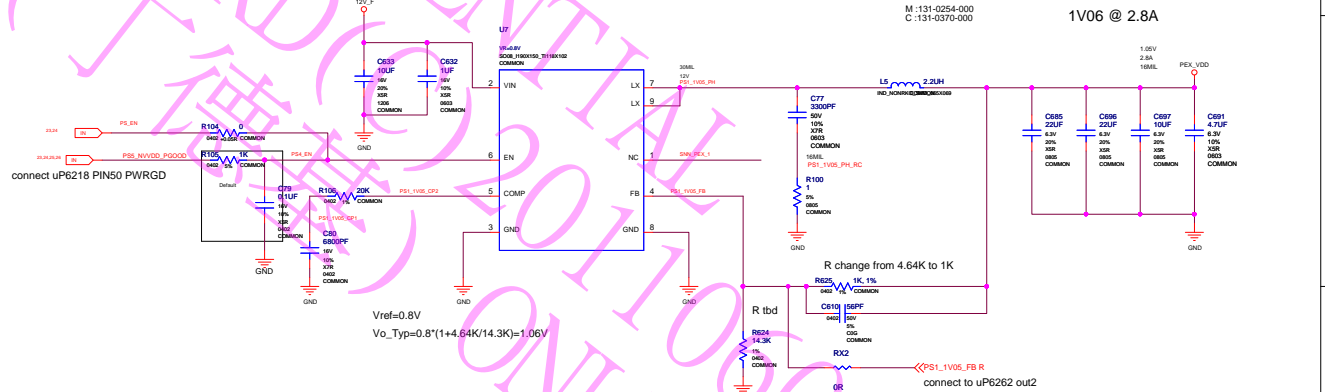
MIO 2V5

2V5 @ 0.8A



PEX_VDD

Input ripple Irms ~0.56A@12V Input

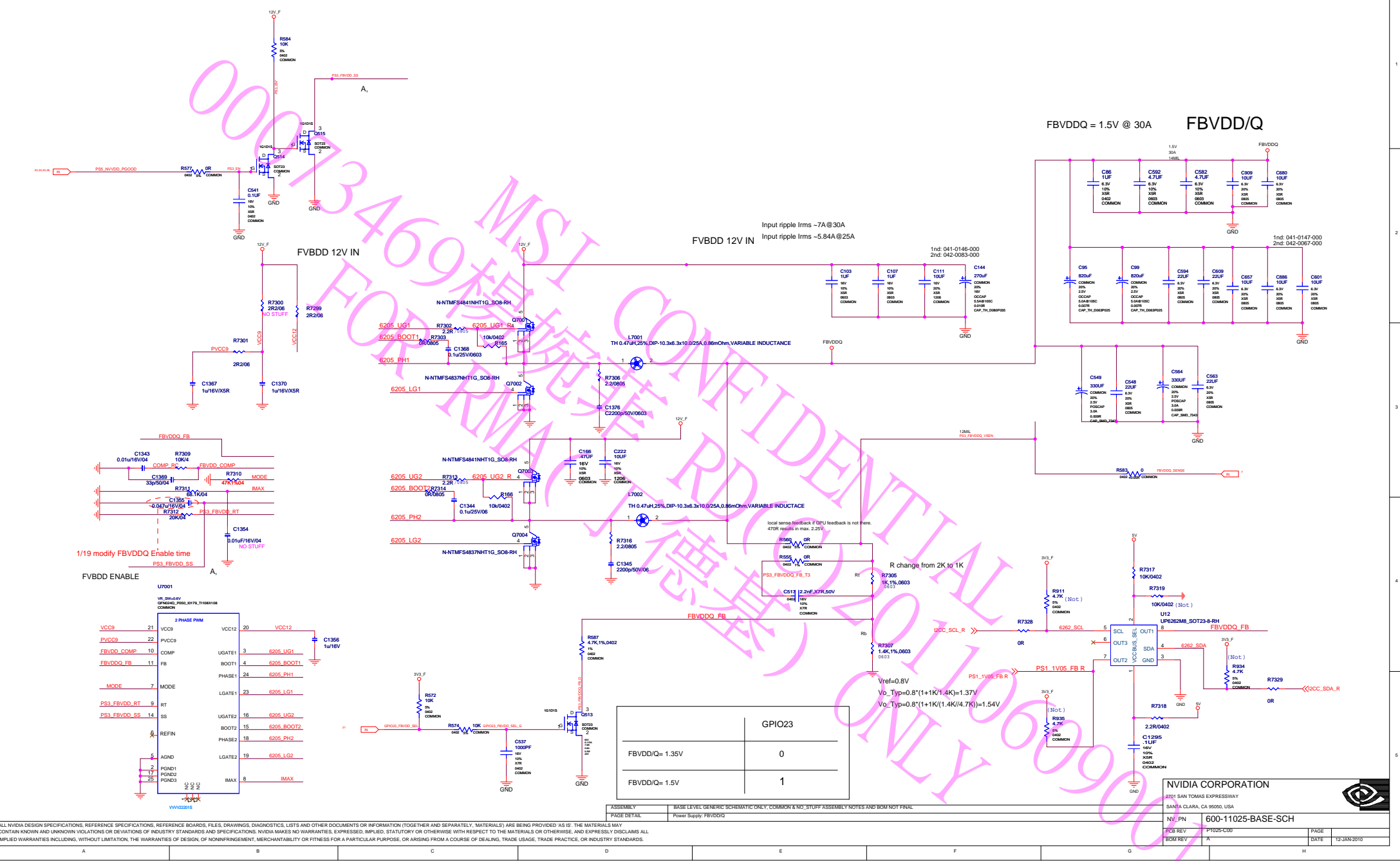


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PAGE DETAIL	Power Supply: 2V5,5V, PEX_VDD

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Power Supply: FBVDDQ

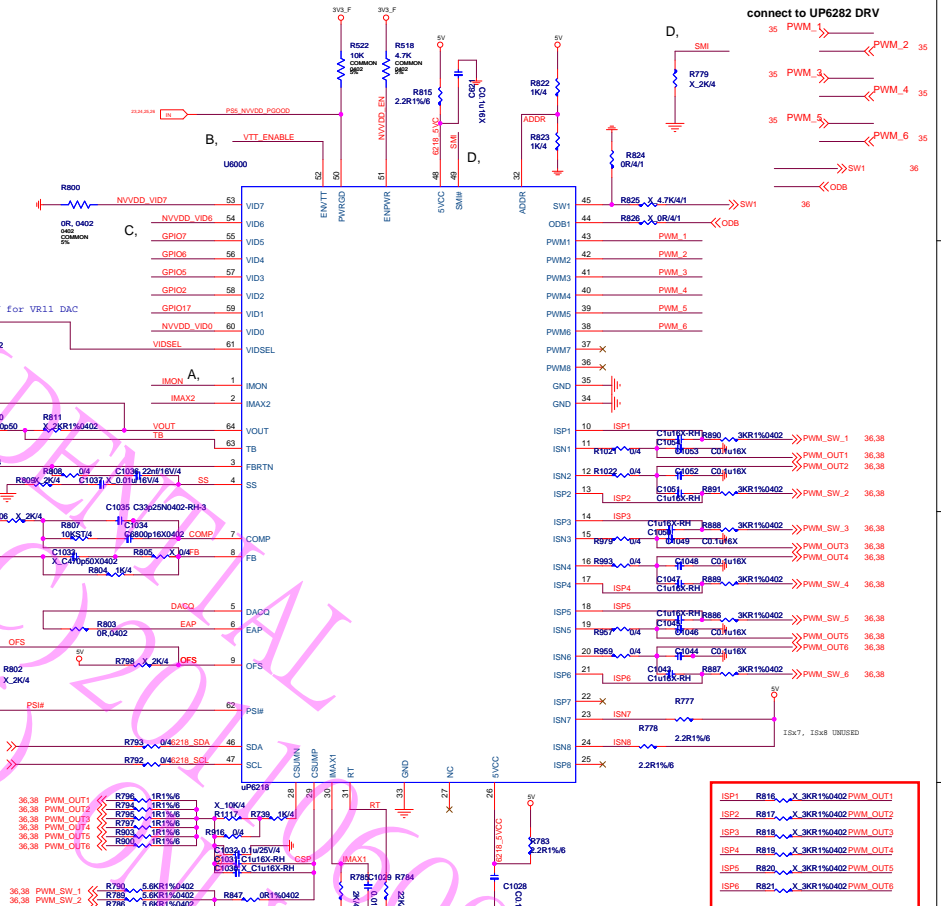
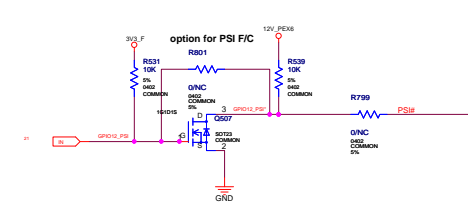
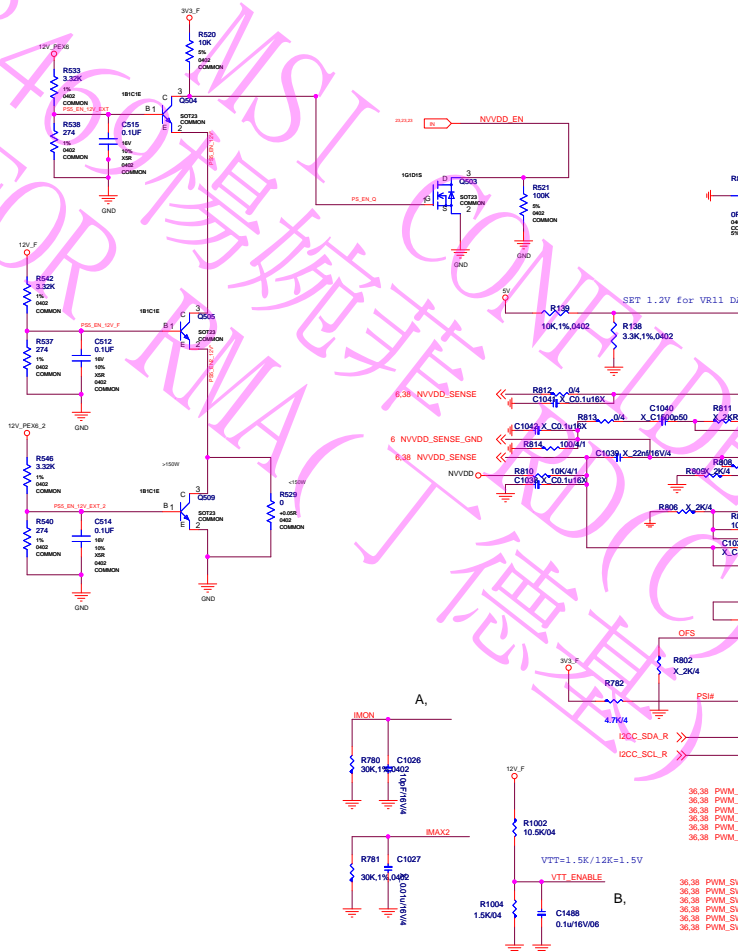
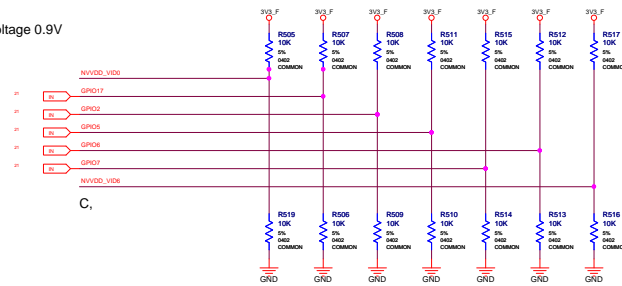


Power Supply: NVVDD Regulator

VID Table

GPI07 VID_5	GPI06 VID_4	GPI05 VID_3	GPI02 VID_2	GPI017 VID_1	VOUT
0	0	0	0	0	1.21250V
0	0	0	0	1	1.20000V
0	0	0	1	0	1.18750V
0	0	0	1	1	1.17500V
0	0	1	0	0	1.16250V
0	0	1	0	1	1.11500V
0	0	1	1	0	1.13750V
0	0	1	1	1	1.12500V
0	1	0	0	0	1.11250V
0	1	0	0	1	1.10000V
0	1	0	1	0	1.08750V
0	1	0	1	1	1.07500V
0	1	1	0	0	1.06250V
0	1	1	0	1	1.05000V
0	1	1	1	0	1.03750V
0	1	1	1	1	1.02500V
1	0	0	0	0	1.01250V
1	0	0	0	1	1.00000V
1	0	0	1	0	0.98750V
1	0	0	1	1	0.97500V
1	0	1	0	0	0.96250V
1	0	1	0	1	0.95000V
1	0	1	1	0	0.93750V
1	0	1	1	1	0.92500V
1	1	0	0	0	0.91250V
1	1	0	0	1	0.90000V
1	1	0	1	0	0.88750V
1	1	0	1	1	0.87500V
1	1	1	0	0	0.86250V
1	1	1	0	1	0.85000V
1	1	1	1	0	0.83750V
1	1	1	1	1	0.82500V

BootVoltage 0.9V



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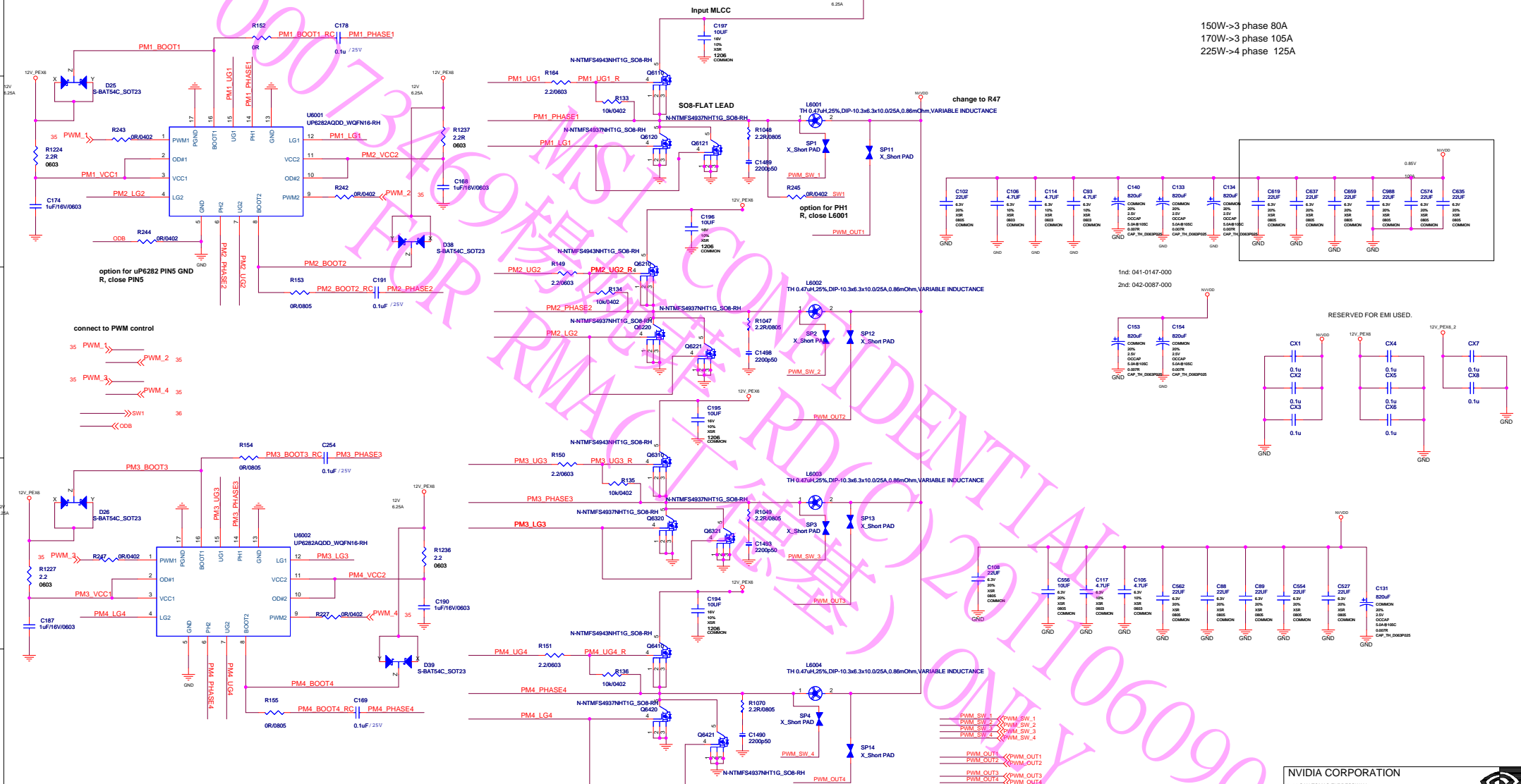
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Power Supply: NVDD Regulator

Power Supply: NVVDD PHASE 1, 2, 3, 4



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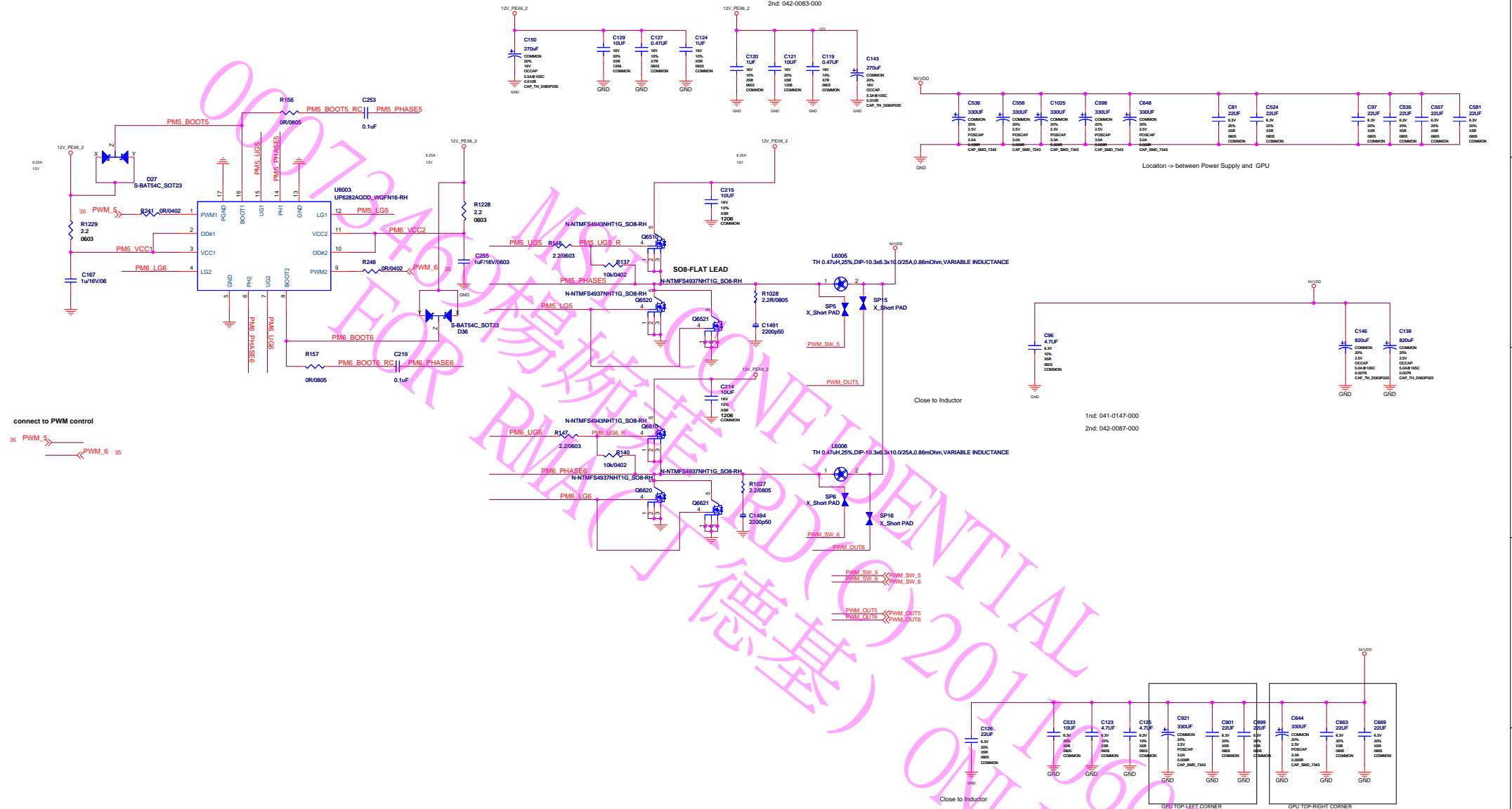
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10. *Journal of the American Medical Association*, 2000; 283: 2689-2694.

Power Supply: NVVDD PHASE 5, 6



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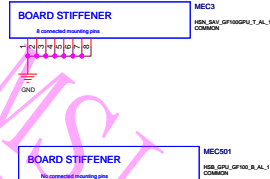
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Bracket and Assembly

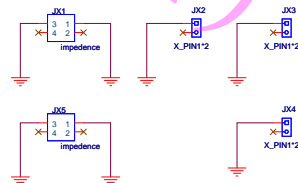
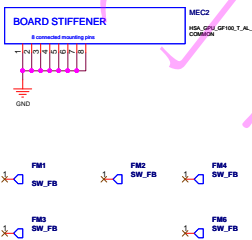
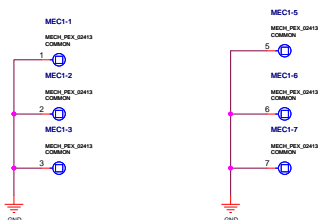
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GPU Stiffener



THERMAL/MECHANICAL HOLES



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